UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,903	10/24/2003	Po-Sheng Shih	250810-1010	8688

24504 7590 05/03/2006

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
100 GALLERIA PARKWAY, NW
STE 1750
ATLANTA, GA 30339-5948

EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,903	SHIH, PO-SHENG	
	Examiner	Art Unit	
	William Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/24/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 9-11, 13-14, 17-18 and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto et al. (US 2002/0047818).

With respect to claim 1, Yamamoto discloses, a black image insertion method for display (para. 37), a black image (note transmittivity in the second half of a vertical scanning period) being inserted between two frames of a liquid crystal display (fig. 14), each of the frames being displayed by a plurality of liquid crystal cells (fig. 18), each of the crystal cells (C_LC in fig. 15) having a first electrode and a second electrode, the first electrode being connected to a switching transistor (TFT_S in fig. 15), a plurality of enable pulses periodically switching the switching transistor (see GL_S applied voltage pulses in fig. 14), the first electrode being connected to a black image electronic element (TFT_C in fig. 15), and the second electrode being connected to a common voltage (CE in fig. 15; para. 86), the black image insertion method comprising:

sending one of the enable pulses (GL_S applied voltage pulse in fig. 14) to switch on the switching transistor, a voltage of the first electrode being changed to a data voltage (potential of PE in fig.14); and

sending a black image enable pulse (GL_C enable pulse in fig. 14) to switch on the black image electronic element before a next enable pulse switches on the switching transistor again, the voltage of the first electrode being changed from the data voltage to a black image voltage (the timing claimed is clear when figs. 14 and 15 are viewed together.).

With respect to claim 2, Yamamoto discloses, the black image insertion method of claim 1 (see above), wherein the black image voltage is between the common voltage plus a zero-level gray scale voltage and the common voltage minus the zero-level gray scale voltage (while Yamamoto does not expressly disclose this limitation; as seen in the potential of PE in fig. 14 the black image voltage is equivalent to the common line voltage. Therefore it is inherent that the black image voltage of Yamamoto is between the range of the common voltage +/- a gray scale voltage, regardless of the value of the gray scale voltage.).

With respect to claim 3, Yamamoto discloses, the black image insertion method of claim 1 (see above), wherein the black image insertion method further comprises: providing an initial voltage to the black image electronic element to turn off the black image electronic element during sending the enable pulse to switch on the switching transistor (note the negative voltage applied during the display period in fig. 14).

With respect to claim 4, Yamamoto discloses, the black image insertion method of claim 3 (see above), wherein the black image insertion method further comprises: returning a voltage of the black image electronic element to the initial voltage after the voltage of the first electrode is changed from the data voltage to the black image voltage (GL_C clearly returns to the initial voltage (2^{nd} negative initial voltage) after the element is supplied with a black voltage).

With respect to claim 5, Yamamoto discloses, the black image insertion method of claim 1 (see above), wherein the black image electronic element comprises a black image transistor (TFT_C in fig. 15).

With respect to claim 6, Yamamoto discloses, the black image insertion method of claim 5 (see above), wherein the black image insertion method further comprises:

providing an initial voltage to the black image transistor to turn off the black image transistor during sending the enable pulse to switch on the switching transistor (note the negative voltage applied during the display period in fig. 14).

With respect to claim 9, Yamamoto discloses, a black image insertion circuit for display, the black image insertion circuit for display comprising:

a switching transistor (TFT_S in fig. 15);

a liquid cell having a first electrode and a second electrode (C_LC in fig. 15);

a scan line switching the switching transistor (GL_S in fig. 15);

a data line sending pixel data to the first electrode through the switching transistor (SL in fig. 15);

a common line (CL in fig. 15), wherein a voltage of the common line is equal to a voltage of the second electrode (para. 86);

a storage capacitor (C_STG in fig. 15) connecting the first electrode and the common line, wherein the storage capacitor stores the pixel data;

a black image transistor (TFT_C in fig. 15), wherein a drain of the black image transistor is connected to the first electrode and a source of the black image transistor is connected to the common line (para. 86); and

a black image line (GL_C in fig. 15), wherein the black image line is connected to a gate of the black image transistor.

With respect to claim 10, Yamamoto discloses, the black image insertion circuit of claim 9 (see above), wherein the black image insertion circuit further comprises a gate driver IC (110 in fig. 17), and the gate driver IC comprises:

at least one first pin connected to the scan line, the first pin sending a first signal to switch the switching transistor (GL_S enable pulse in fig. 14); and

at least one second pin connected to the black image line, the second pin sending a second signal to switch the black image transistor (GL_C enable pulse in fig. 14), wherein a predetermined time offset exists between the first signal and the second signal (note the time offset between the two enable pulses in fig. 14).

With respect to claim 11, Yamamoto discloses, the black image insertion circuit of claim 10 (see above), wherein periods of the first signal and the second signal are equal (clear from fig. 14).

With respect to claim 13, Yamamoto discloses, a black image insertion circuit for display, the black image insertion circuit for display comprising;

a switching transistor(TFT_S in fig. 15);

a liquid cell having a first electrode and a second electrode (C_LC in fig. 15), wherein a voltage of the second electrode is equaled to a common voltage (para. 86);

a scan line switching of the switching transistor (GL_S in fig. 15);

a data line sending pixel data to the first electrode trough the switching transistor (SL in fig. 15);

a black image electronic element (TFT_C in fig. 15), wherein the black image electronic element is connected to the first electrode (para. 86);

a black image line sending a black image data to the first electrode through the black image electronic element (GL_C in fig. 15); and

a storage capacitor connecting the first electrode and the black image line, wherein the storage capacitor stores the pixel data (C_STG in fig. 15).

With respect to claim 14, Yamamoto discloses, the black image insertion method of claim 13 (see above), wherein the black image electronic element comprises a black image transistor (TFT_C in fig. 15).

With respect to claim 17, Yamamoto discloses, the black image insertion circuit of claim 13 (see above), wherein the black image insertion circuit further comprises a gate driver IC (110 in fig. 17), and the gate driver IC comprises:

at least one first pin connected to the scan line, the first pin sending an enable signal to switch the switching transistor (GL_S enable pulse in fig. 14); and

at least one second pin connected to the black image line, the second pin sending the black image data to the black image line (GL_C enable pulse in fig. 14), wherein a predetermined time offset exists between the first signal and the second signal (note the time offset between the two enable pulses in fig. 14).

With respect to claim 18, Yamamoto discloses, the black image insertion circuit of claim 17 (see above), wherein periods of the enable signal and the black image data are equal (clear from fig. 14).

With respect to claim 20, Yamamoto discloses, a gate driver IC (110 in fig. 17) for a liquid crystal display, driving at least one liquid crystal pixel (C_LC in fig. 15), the liquid crystal pixel having a switching transistor (TFT_S in fig. 15) and a black image line (GL_C in fig. 15), the gate driver IC for a liquid crystal display comprising:

at least one first pin connected to a gate of the switching transistor, wherein the first pin sends a first signal to switch the switching transistor (GL_S enable pulse in fig. 14); and

at least one second pin connected to the black image line, wherein the second pin sends a second signal to the black image line to display a black image on the crystal pixel (GL_C enable pulse in fig. 14), and wherein a predetermined time offset exists between the first signal and the second signal (note the time offset between the two enable pulses in fig. 14).

With respect to claim 21, Yamamoto discloses, the black image insertion circuit of claim 20 (see above), wherein periods of the enable signal and the black image data are equal (clear from fig. 14).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US 2002/0047818) in view of Ono et al. (US 5,526,013).

With respect to claims 12, 19 and 22, Yamamoto discloses, the black image insertion circuit of claims 10, 17 and 20 (see above).

Yamamoto does note expressly disclose, wherein periods of the first signal and the second signal are unequal.

Ono discloses, wherein periods of a reset enable pulse and a data enable pulse are unequal (col. 22, lines 43-61).

Ono and Yamamoto are analogous art because they are both from the same field of endeavor namely driving waveforms for LCD displays.

At the time of the invention it would have been obvious to one of ordinary skill in the art to alter the timing of the reset pulses of Yamamoto as taught by Ono.

The motivation for doing so would have been to lessen the degradation of the display quality (Ono; col. 2, lines 53-54).

Therefore it would have been obvious to combine Ono with Yamamoto for the benefit of a higher quality display to obtain the invention as specified in claims 12, 19 and 22.

6. Claims 7-8 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US 2002/0047818) in view of Yi et al. (US 6,791,522).

With respect to claim 7, Yamamoto discloses, the black image insertion method of claim 6 (see above).

Yamamoto does not expressly disclose, wherein when a source and a gate of the black image transistor are connected to the initial voltage and a drain of the black image transistor is connected to the first electrode, the initial voltage is lower than the data voltage and the black image enable pulse is higher than the data voltage.

Yi discloses, a diode (D3 in fig. 3) connected to a reset line and an electrode (Cl in fig. 3). As disclosed by the Applicant (page 14, lines 24-25) a diode in this orientation is an equivalent circuit to the transistor limitations described in the current claim (also note col. 3, lines 60-61 of Yi). Further, Yi discloses, that the reset diode (D3 in fig. 3) is turned on to discharge the load capacitor (col. 3, lines 9-11). This inherently requires certain voltage comparisons; namely that the initial voltage is lower than the data voltage and the black image enable pulse is higher than the data voltage.

Yi and Yamamoto are analogous art because they are both from the same field of endeavor namely LCD display pixel circuitry and driving.

At the time of the invention it would have been obvious to one of ordinary skill in the art to rewire the black image transistor of Yamamoto as taught by Yi.

The motivation for doing so would have been a both an easier and cheaper method of manufacture (Yi; col. 2, lines 1-4).

Therefore it would have been obvious to combine Yi with Yamamoto for the benefit an easier method of manufacture to obtain the invention as specified in claim 7.

With respect to claim 8, Yamamoto discloses, the black image insertion method of claim 6 (see above).

Yamamoto does not expressly disclose, wherein when a source and a gate of the black image transistor are connected to the first electrode and a drain of the black image transistor is connected to the initial voltage, the initial voltage is higher than the data voltage and the black image enable pulse is lower than the data voltage.

Yi discloses, a diode (D3 in fig. 2) connected to a reset line and an electrode (Cl in fig. 2). As disclosed by the Applicant (page 18, lines 18-19) a diode in this orientation is an equivalent circuit to the transistor limitations described in the current claim (also note col. 3, lines 60-61 of Yi). Further, Yi discloses, that the reset diode (D3 in fig. 2) is turned on to discharge the load capacitor (col. 3, lines 9-11). This inherently requires certain voltage comparisons; namely that the initial voltage is lower than the data voltage and the black image enable pulse is higher than the data voltage.

For motivation and further merits of the rejection see the above rejection of claim 7.

With respect to claim 15, Yamamoto discloses, the black image insertion method of claim 14 (see above).

Yamamoto does not expressly disclose, wherein when a source and a gate of the black image transistor are connected to the initial voltage and a drain of the black image transistor is connected to the first electrode.

Yi discloses, a diode (D3 in fig. 3) connected to a reset line and an electrode (CI in fig. 3). As disclosed by the Applicant (page 14, lines 24-25) a diode in this orientation is an equivalent circuit to the transistor limitations described in the current claim (also note col. 3, lines 60-61).

Yi and Yamamoto are analogous art because they are both from the same field of endeavor namely LCD display pixel circuitry and driving.

At the time of the invention it would have been obvious to one of ordinary skill in the art to rewire the black image transistor of Yamamoto as taught by Yi.

The motivation for doing so would have been a both an easier and cheaper method of manufacture (Yi; col. 2, lines 1-4).

Therefore it would have been obvious to combine Yi with Yamamoto for the benefit an easier method of manufacture to obtain the invention as specified in claim 15.

With respect to claim 16, Yamamoto discloses, the black image insertion method of claim 14 (see above).

Yamamoto does not expressly disclose, wherein when a source and a gate of the black image transistor are connected to the first electrode and a drain of the black image transistor is connected to the black image line.

Yi discloses, a diode (D3 in fig. 2) connected to a reset line and an electrode (CI in fig. 2). As disclosed by the Applicant (page 18, lines 18-19) a diode in this orientation is an equivalent circuit to the transistor limitations described in the current claim (also note col. 3, lines 60-61 of Yi).

For motivation and further merits of the rejection see the above rejection of claim 15.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wlb
4/26/06

AMR A. AWAD
PRIMARY EXAMINER